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ISL75052SEH PSPICE Macro-Model

Introduction

The ISL75052SEH is a radiation hardened, single output LDO specified for an output current of 1.5A. The device operates from an input voltage range of 4.0V to 13.2V and provides for output voltages of 0.6V to 12.7V. The output is adjustable based on a resistor divider setting. Dropout voltages as low as 75mV (at 0.5A) typical can be realized using the device. This allows the user to improve the system efficiency by lowering V_{IN} to nearly V_{OUT}.

The SPICE model for the ISL75052SEH was developed to help system designers evaluate the operation of this IC prior or in conjunction with proto-typing a system design. This model accurately simulates typical performance characteristics at room temperature (+25°C) such as frequency analysis, steady state analysis, and transient analysis. Behaviors not supported are the bias current cancellation circuit and some temperature analysis. Functionality has been tested on ORCAD 10.0 and CADENCE ORCAD 16.5. Other SPICE simulators may be used, however, the model may require translation.

Reference Documents

- ISL75052SEH Data Sheet; FN8456
- ISL75052SEH SMD 5962-13220

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Project Files

The zip file: **ISL75052SEH.zip** contains the project file ISL75052SEH.opj to be used in ORCAD simulator. The project file has the model definition file (.lib), symbol file (.olb) and various design files (.dsn) to simulate start up, OCP, load transients, etc. The application circuit is shown in Figure 1. Figures 2 through 9 show a comparison of the simulation results versus bench results for various tests. The close agreement between model and actual measurement demonstrate the accuracy of the model, making it a very powerful tool.

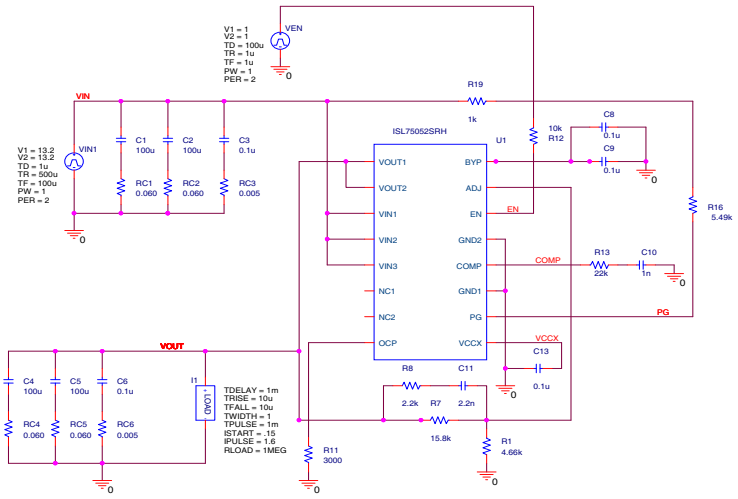

FIGURE 1. ISL75052SEH PSPICE SCHEMATIC

Simulation Performance Curves

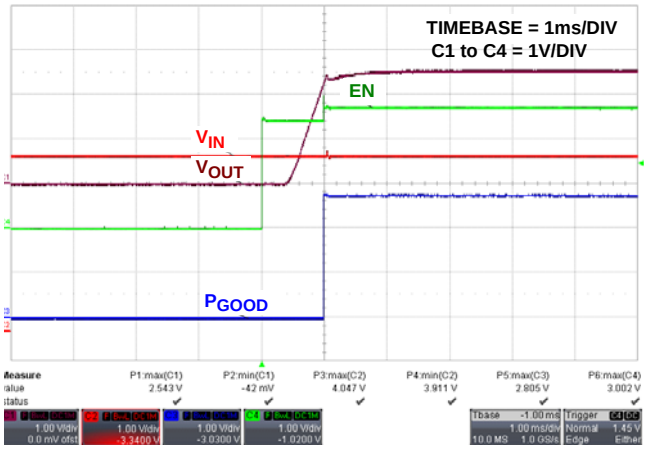

FIGURE 2. +25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

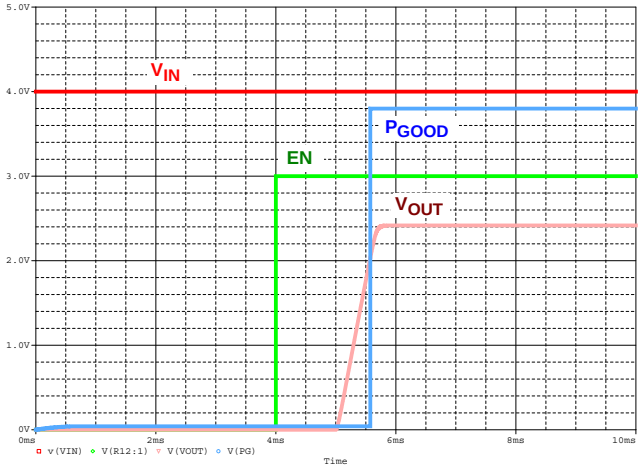

FIGURE 3. SIMULATED +25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

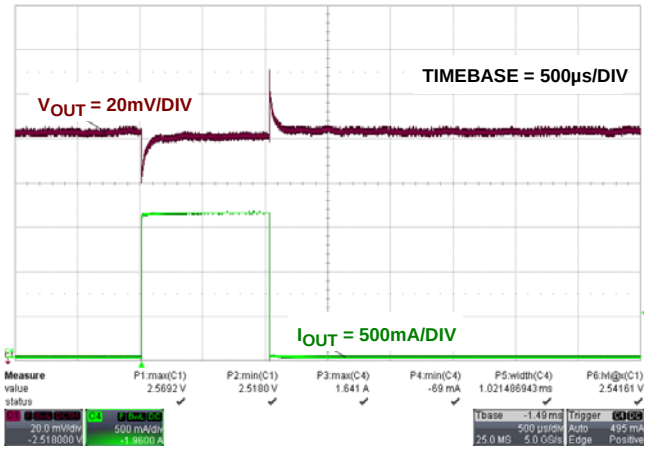

FIGURE 4. LOAD STEP RESPONSE, +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.15A TO 1.6A, C_{OUT} = 200µF, 30mΩ

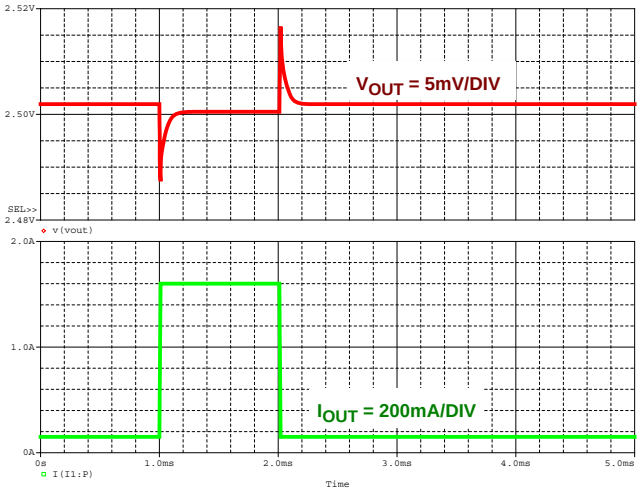

FIGURE 5. SIMULATED LOAD STEP RESPONSE, +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.15A TO 1.6A, C_{OUT} = 200µF, 30mΩ

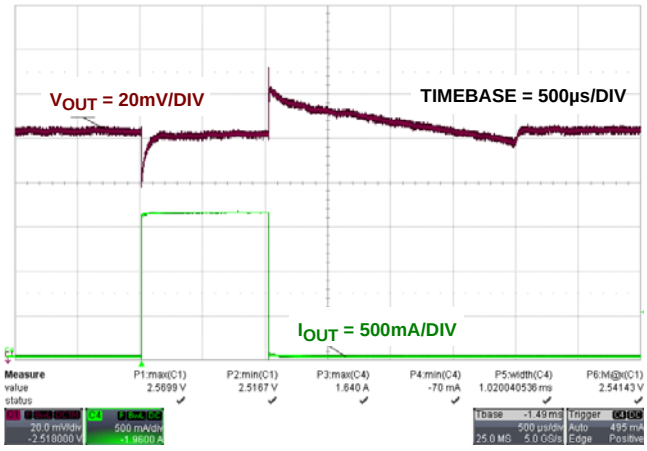

FIGURE 6. LOAD STEP RESPONSE +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0A TO 1.6A, C_{OUT} = 200µF, 30mΩ

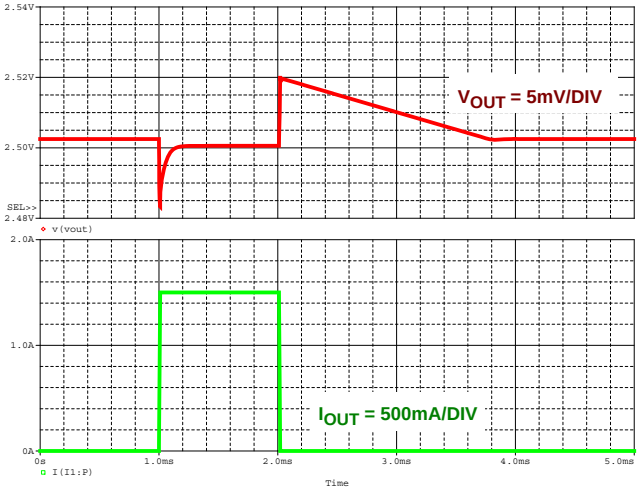

FIGURE 7. SIMULATED LOAD STEP RESPONSE +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0A TO 1.6A, C_{OUT} = 200µF, 30mΩ

Simulation Performance Curves (Continued)

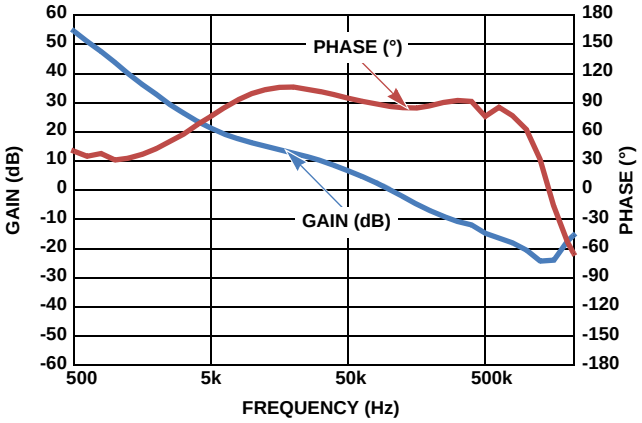

FIGURE 8. GAIN PHASE PLOTS, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 84.56°, GAIN MARGIN = 18.06dB

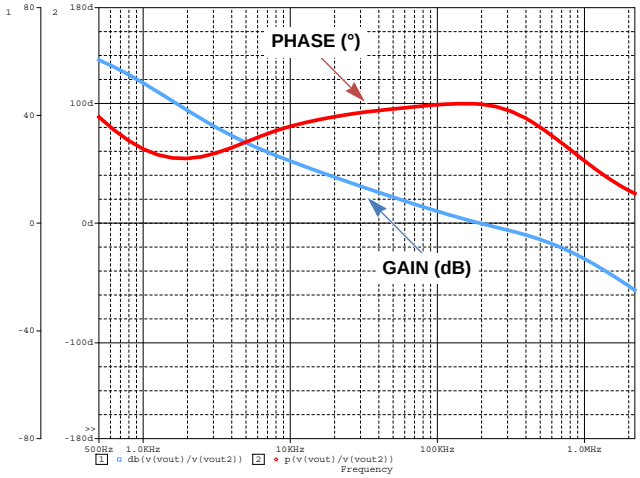

FIGURE 9. SIMULATED GAIN PHASE PLOTS, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 84.56°, GAIN MARGIN = 18.06dB